Netlist Viewer User Guide

Libero SoC v2023.1

Introduction (Ask a Question)

As Field Programmable Gate Array (FPGA) designs grow in size and complexity, it has become essential for FPGA designers to traverse the netlist to analyze their designs. The Microchip Netlist Viewer is a graphical representation of the design netlist that displays different views for the different stages of the design process.

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1. Supported Families and Platforms (Ask a Question)

The Netlist Viewer supports SmartFusion® 2, IGLOO® 2, RTG4™, PolarFire®, and PolarFire SoC family devices and runs on Windows® and Linux® systems.

Note: Depending on the device selected, some user interface elements such as icons, options, tabs, and dialog boxes may vary slightly in appearance and/or content. Basic Netlist Viewer functionality remains the same, regardless of the device chosen. In this user guide, a PolarFire device is used in the example figures.

2. Views (Ask a Question)

The Netlist Viewer is a Graphical User Interface (GUI) that displays different views for the different stages of the design process:

- Register Transfer Level (RTL) Netlist view—shows how the Verilog code appears in design format. Using this view, you can confirm whether software implemented the correct logic. Cross probing between this view and the HDL code aids in troubleshooting when the design does not work as desired.
- Hierarchical Post-Synthesis view—hierarchical view of the netlist after synthesis and after technology mapping to the Microchip FPGA technology.
- Flat Post-Compile Netlist view—a flattened netlist after synthesis, technology mapping and further optimization based on the Design Rules Check (DRC) rules of the device family and/or die.
- Flat Post-Compile Cone view—loads the same netlist as the Flat Post-Compile view, but does not initially draw anything on the canvas. Important parts of the design can be added to the canvas from the tree or from the existing items in the view. This view opens much more quickly than the Flat Post-Compile view. It allows you to load only the parts of the design you are interested in. This view is well-suited for use with large designs. This view is not available for all families.

Figure 2-1. Netlist Viewer—RTL View

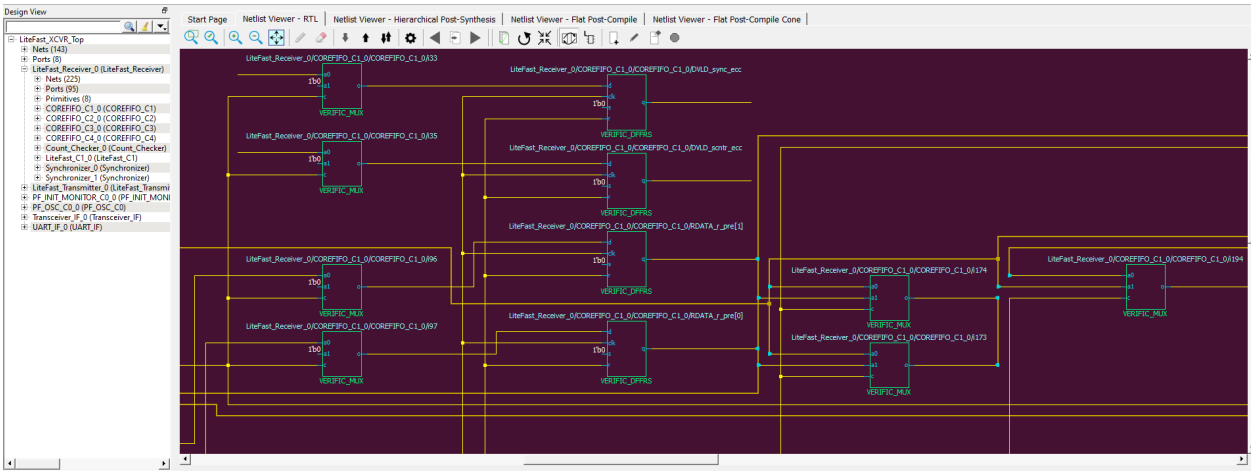


Figure 2-2. Netlist Viewer—Hierarchical Post-Synthesis View

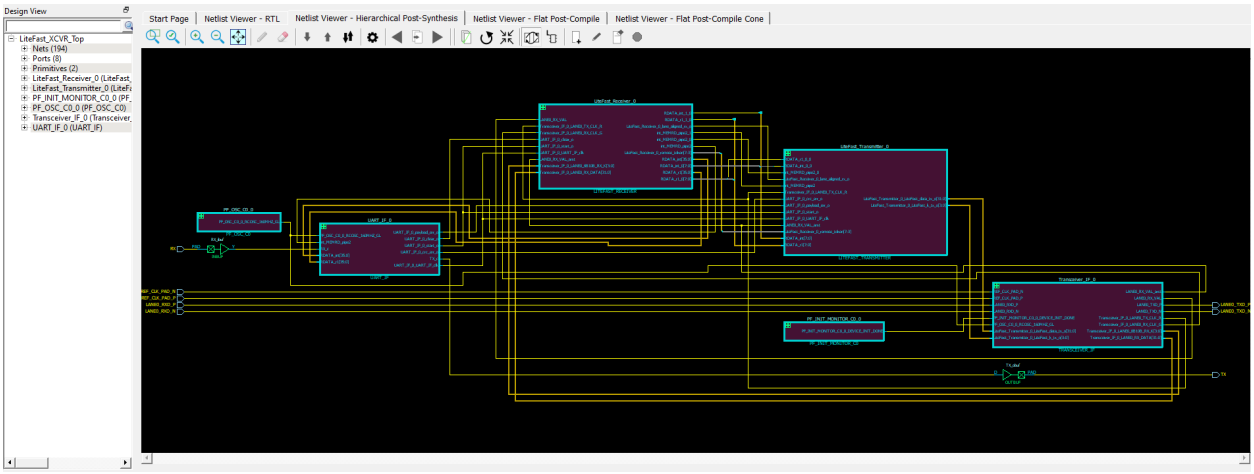
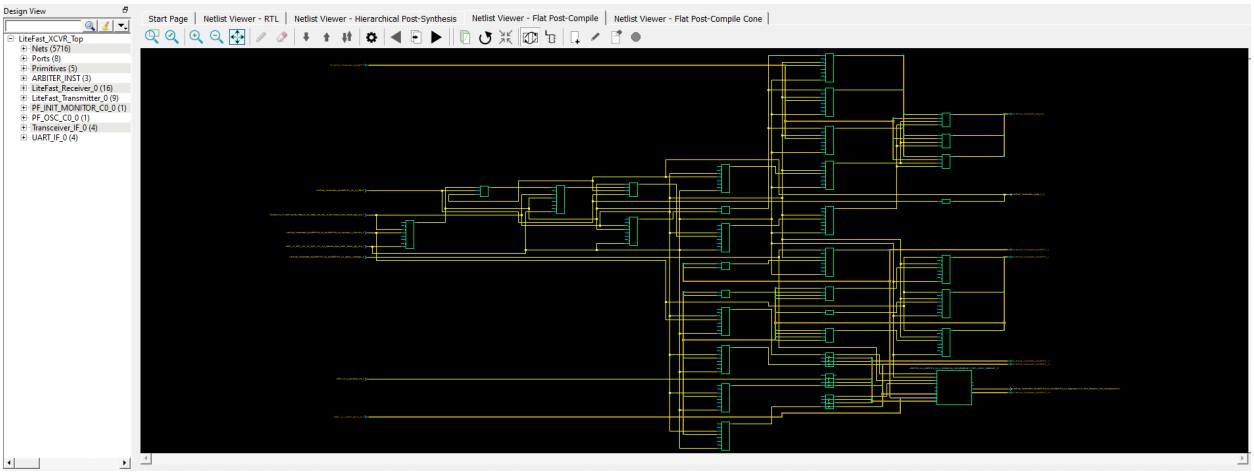
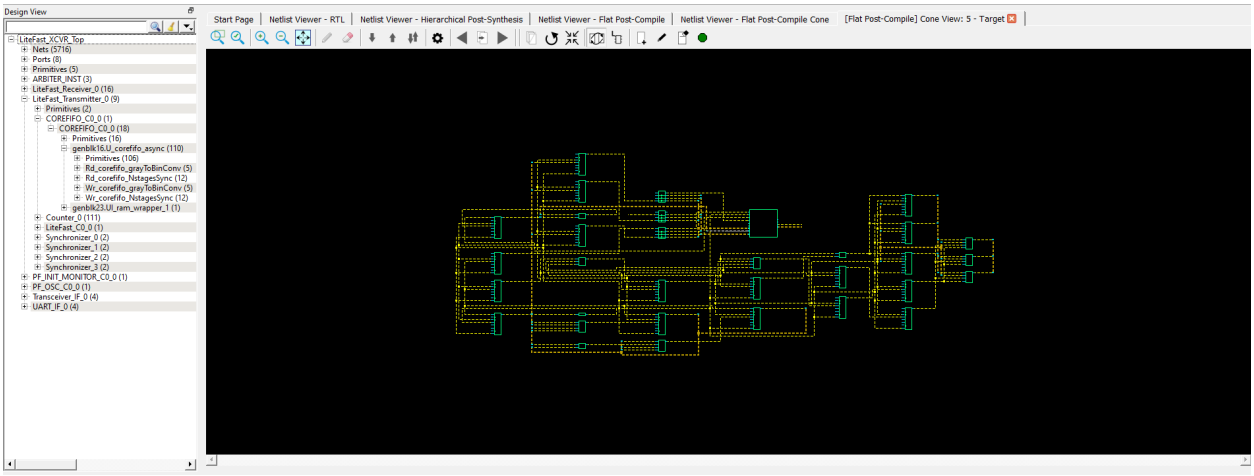


Figure 2-3. Netlist Viewer—Flat Post-Compile View



Important: A progress bar indicates that the flattened netlist is being loaded. For a large netlist, the loading may incur some runtime penalty. A **Cancel** button is available to cancel the loading.

Figure 2-4. Netlist Viewer—Flat Post-Compile Cone View

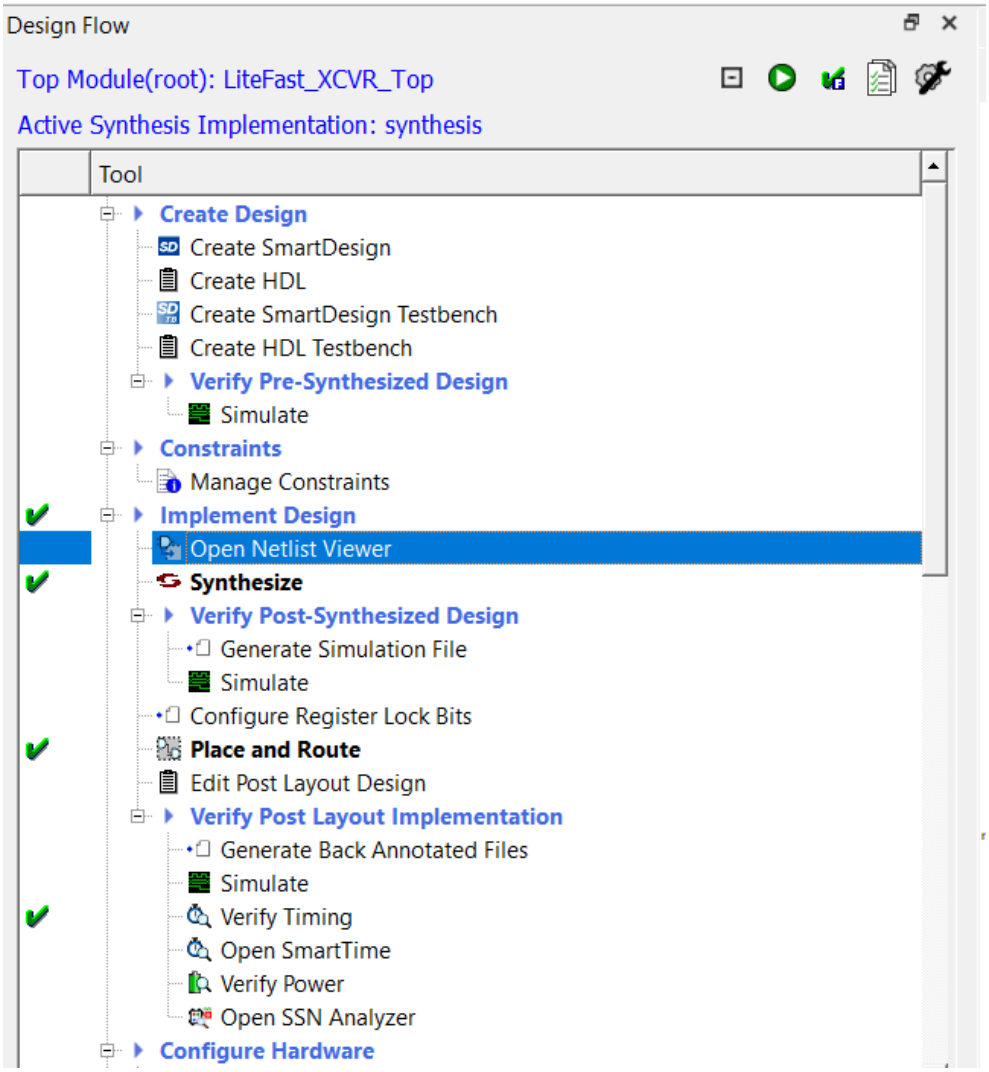


3. Invocation (Ask a Question)

The standalone Netlist Viewer is available for invocation in the Design Flow window. To open the standalone Netlist Viewer in the Flow window, perform one of the following steps:

- Double click **Netlist Viewer** in the Design Flow window
- Right click **Netlist Viewer** and select **Open Interactively**

Figure 3-1. Netlist Viewer Invocation—Design Flow Window



When Netlist Viewer opens, it makes available for loading and viewing the following views of the netlist:

- RTL—available after design capture/design generation
- Hierarchical Post-Synthesis—available after Synthesis
- Flat Post-Compile—available after Synthesis or Place and Route. If after Place and Route, the Netlist Viewer loads the Flat Post-Compile view to reflect the netlist generated after Place and Route.
- Flat Post-Compile Cone—available after Synthesis or Place and Route. If after Place and Route, the Netlist Viewer loads the Flat Post-Compile view to reflect the netlist generated after Place and

Route. This view does not display any netlist on the canvas until an instance from the design tree is selected and loaded. This view allows you to load in a special area of the design in which you are interested. It also cuts down the runtime.

4. Netlist Viewer Windows (Ask a Question)

When the standalone Netlist Viewer opens, no netlist views are loaded. The Start Page shows the netlist views that can be opened for viewing.

The Netlist Viewer User Guide is available from the Design Flow window (**Netlist Viewer** > **Help** > **Netlist Viewer User Guide**) and also from the Help menu (**Help** > **Reference Manuals**).

4.1 Opening a View (Ask a Question)

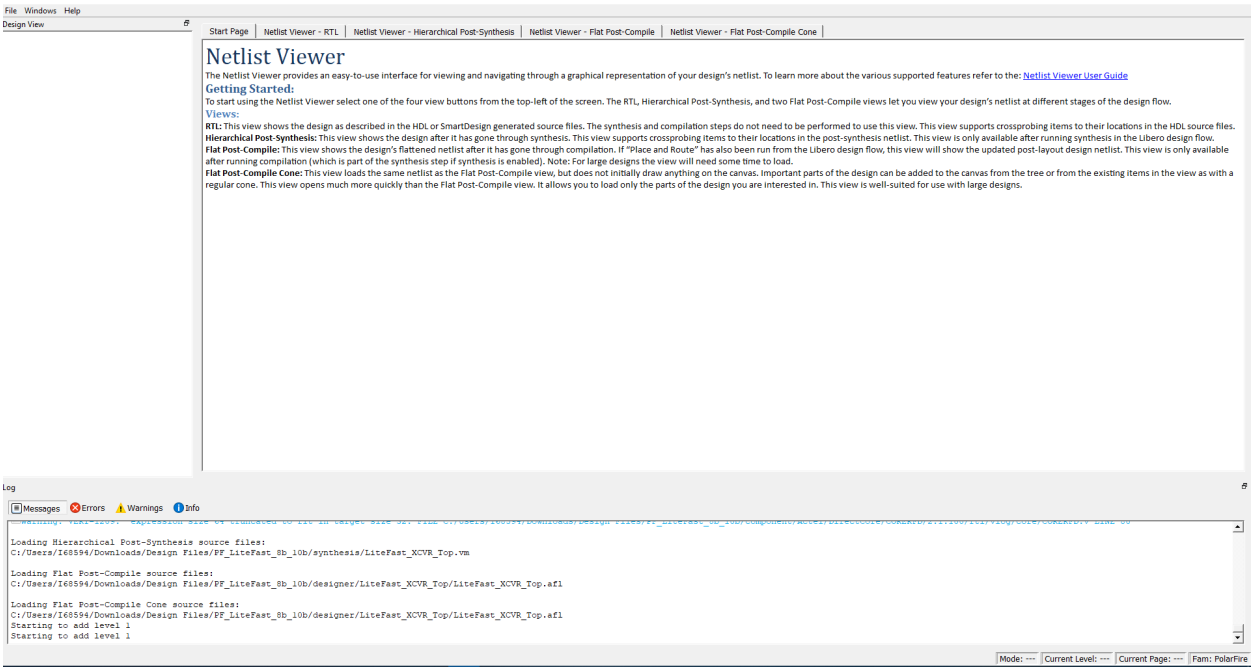
Click any of the following views at the top-left corner to load the netlist into the Netlist Viewer for viewing:

- RTL view—pre-synthesis RTL netlist is drawn in the view
- Hierarchical Post-Synthesis view—post-synthesis netlist is drawn in the view

Note: The Hierarchical Post-Synthesis view is not available if synthesis is disabled in the design flow (**Project** > **Project Settings** > **Design Flow** > **Enable Synthesis** is unchecked).

- Flat Post-Compile view—flattened post-compile netlist is drawn in the view
- Flat Post-Compile Cone view—no netlist is drawn until design objects are added to the view

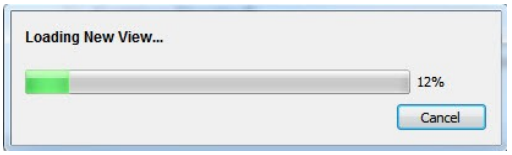
Figure 4-1. Netlist Viewer on Start Up



Important:

- When you open netlist views for the first time in the Netlist Viewer, they load into system memory, where they remain until the Netlist Viewer exits. For very large designs, loading the netlist for the first time may take some time. A pop-up window reports the status of the loading process.
- The Flat Post-Compile Cone view takes very little runtime because no netlist is drawn when this view is first loaded. This view does not display a netlist until instances from the design tree are selected and loaded.

Figure 4-2. Loading New View Popup Window

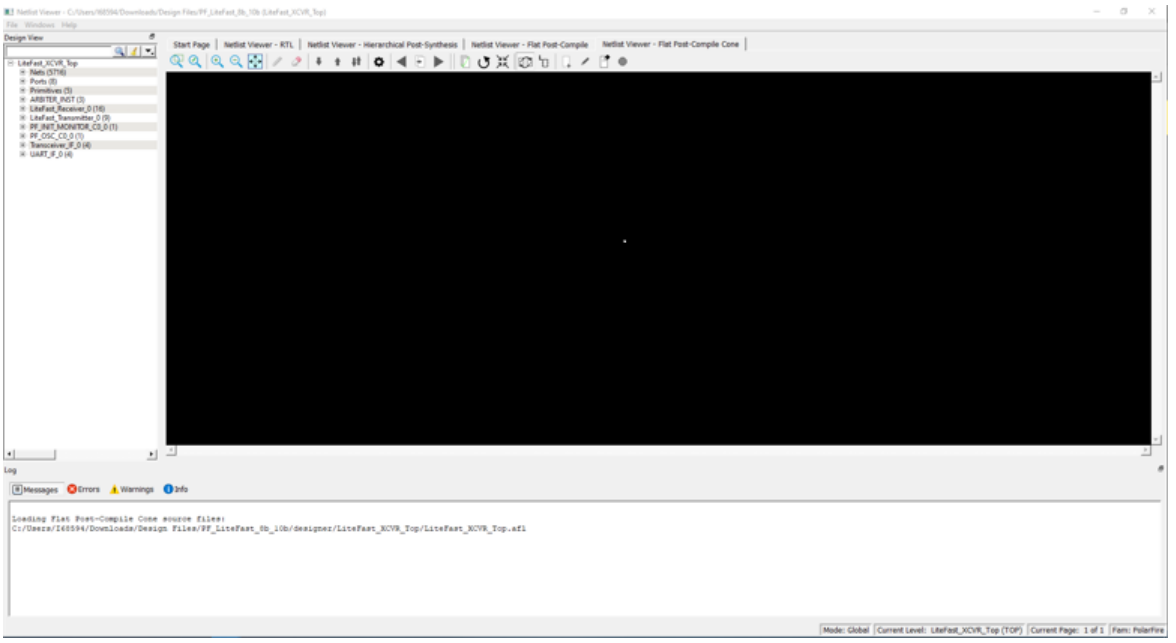


After the netlist views open for the first time, they load into system memory, making them available almost immediately in the Netlist Viewer.

4.1.1 Displaying the Flat Post-Compile Cone View (Ask a Question)

When the Flat Post-Compile Cone view has finished loading, unlike the other three views, nothing is drawn in the canvas.

Figure 4-3. Flat Post-Compile Cone View when Loaded—No Design Object Added



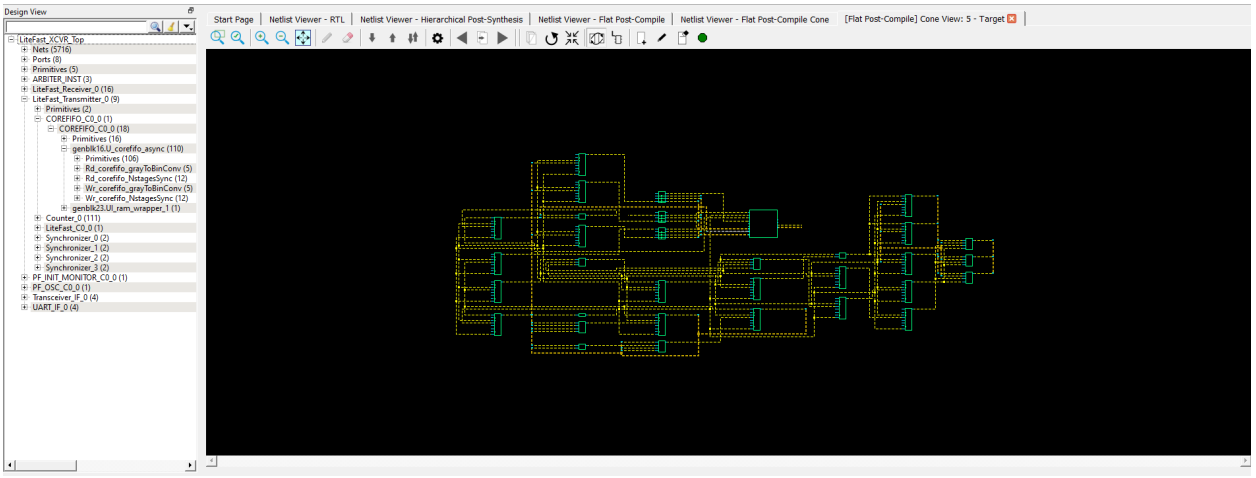
This view is useful when a small or critical part of a very large design needs to be examined. Design objects that can be selected for display in this view include:

- Nets
- Ports
- Macros
- Components

To display design objects in the Flat Post-Compiled Cone view, right click the design object (**Nets, Macro, Ports, or Component**) in the Design Tree and select **Load Selection**. The design object is added to the view.

Opening a design in the Flat Post-Compile view may incur a runtime penalty. This cone view loads the same AFL netlist source file as the Flat Post-Compile view. However, this cone view, unlike the Flat Post-Compile view, draws nothing until you select a part of the design you want to display. This reduces the runtime penalty associated with drawing a large netlist for display.

Figure 4-4. Flat Post-Compile Cone View—Design Objects Added

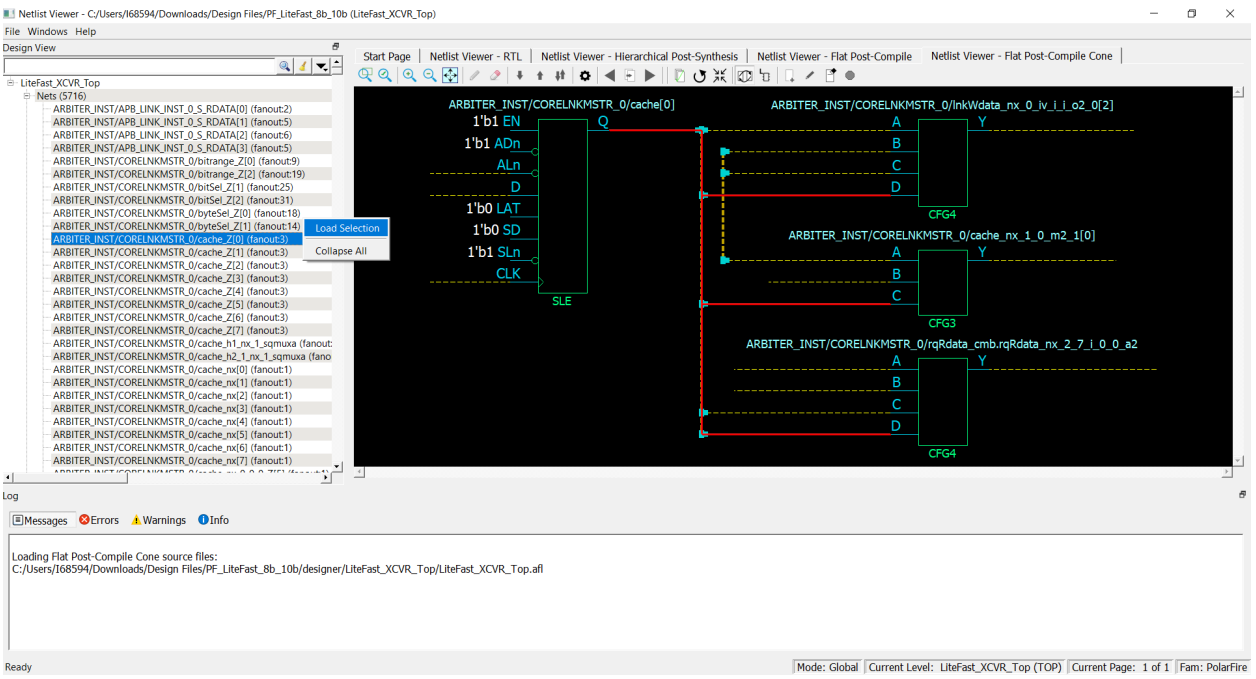


4.1.1.1 Adding a Net (Ask a Question)

Right click a net in the Design Tree and select **Load Selection** to add a net to the view. Adding a net to the view adds a solid line net to the view (unless you cancel early), including all the instances and ports the net is connected to. The added net is selected in the view.

Nets that span multiple pages can be followed through the right click menu item **Follow Net to Page#** to go to different pages that the net is on.

Figure 4-5. Net Added to View — Solid Line

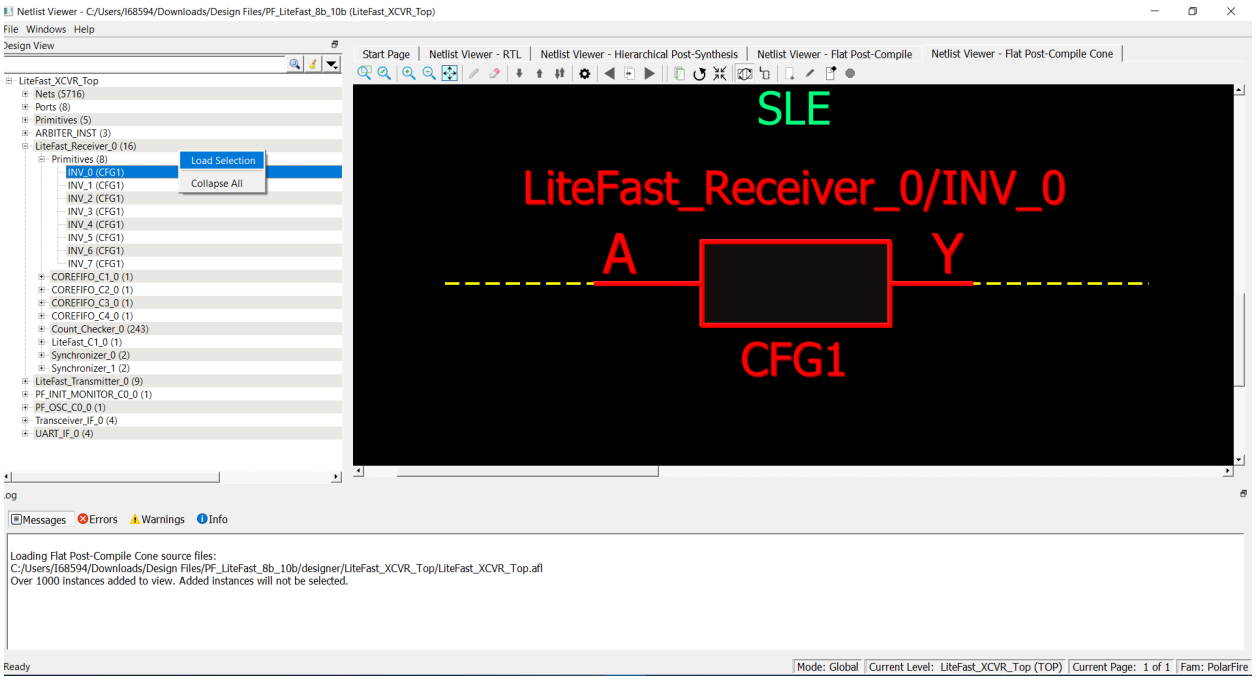


4.1.1.2 Adding a Macro (Ask a Question)

A macro is a basic low-level design object from the Macro Library in the Catalog. Right click a macro in the Design Tree and select **Load Selection**to add a macro. Adding a macro adds the instance with its connected nets to the view. The connected nets are always dashed yellow lines, even if they are not connected to any logic outside the view. Double clicking the net adds connections (if any) and

turns the net from a dashed line to a solid line. A solid line for a net indicates that it is a user-added net.

Figure 4-6. CFG4 Macro Added



4.1.1.3 Adding a Port (Ask a Question)

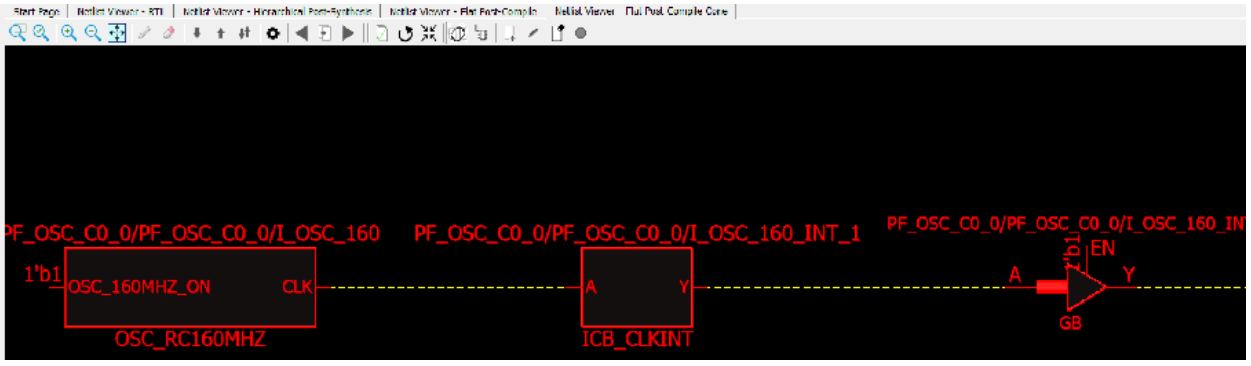
To add a port to the view, right click a port in the Design Tree and select **Load Selection**. Adding a port to the view is the same as adding a net connected to the port.

4.1.1.4 Adding a Component (Ask a Question)

Right click a component in the Design Tree and select **Load Selection** to add a component to the view. Adding a component to the view is the same as selecting all lower level macros and adding them to the view. The added macros are selected.

Important: To save runtime for very large components with many low level macros, the macros are added, but cannot be selected.

Figure 4-7. Component Added



4.1.1.5 Load/Driver Display (Ask a Question)

Design objects can also be added to the view through the right click menu to add load/driver. This action adds any instances at the different logical levels.

4.2 Closing a View (Ask a Question)

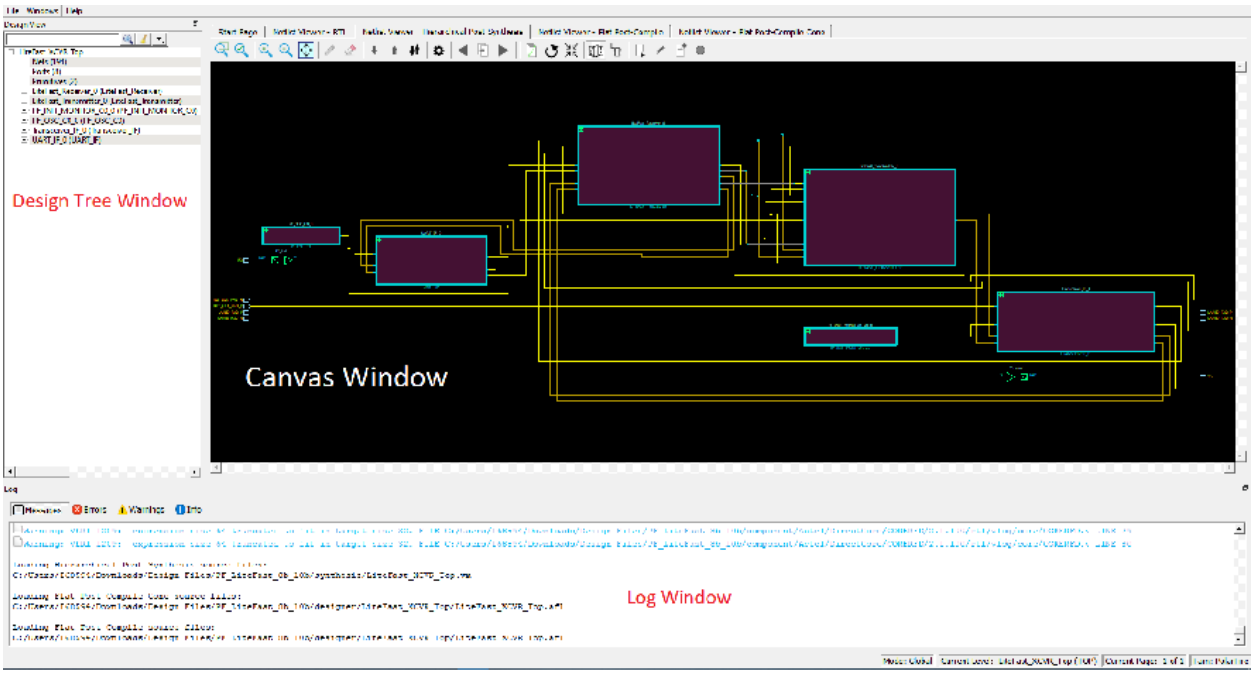
To close the opened view, click an opened view at the top of the Netlist Viewer. A closed view stays in system memory as long as the Netlist Viewer remains open. Opening the same netlist view at a later time does not incur runtime penalty, as no loading is required.

4.3 Netlist Viewer Windows (Ask a Question)

When the Netlist Viewer opens, it displays three windows by default.

- Design Tree window displays the design hierarchy from the top level.
- Canvas window displays the netlist views.
- Log window displays messages, warnings, info, and so on.

Figure 4-8. Netlist Viewer Windows



4.4 Design Tree Window (Ask a Question)

The Design Tree window displays the design hierarchy from the top level. By default, when the Netlist Viewer opens, it displays the Design Tree window.

Note: The Design Tree window is displayed by default when the Netlist Viewer opens. Hiding the Design Tree view will leave more display area for the Canvas view. To get a bigger display area for the canvas view, hide the Design Tree window (**Netlist Viewer > Windows** and uncheck **Show Tree**)
The Design Tree window displays:

- Nets (<integer>)—number in brackets is the total number of nets at the top level
- Ports (<integer>)—number in brackets is the total number of ports at the top level
- Design components under the top level—each component can be collapsed or expanded to expose
  - Nets—total number of nets at the component level
  - Ports—total number of ports at the component level

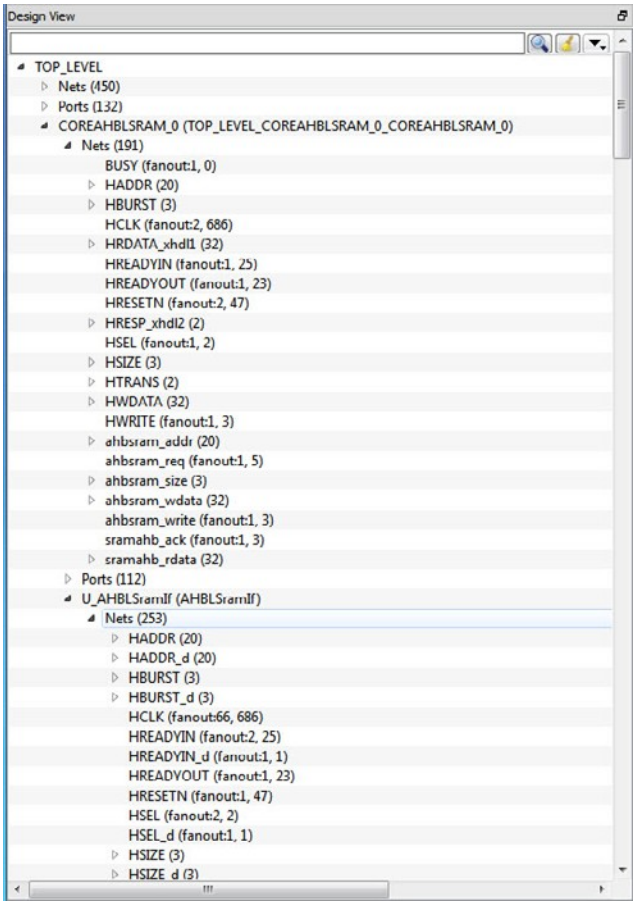
  - Subcomponents inside the component

- Fanout Values (Nets)—when two numbers are displayed in the bracket, the first number is the fanout of the net at the local level (of hierarchy) and the second number is the fanout of the net at the global level. As an example, net_xyz (fanout: 1,3) means the net goes down the levels of hierarchy to three different pins (global fanout 3) and is not connected to any other pins at the current level (local fanout 1).
- Primitives—primitives refer to macros and low-level design objects and can appear in the top level or component level.

The design tree is different with different netlist views. For the Flat Post-Compile view, the design tree displays a much larger number of nets than the RTL view or Hierarchical Post-Synthesis view, because the netlist is flattened in the Post-Compile view and all nets are counted. The nets in the Flat Post-Compile view, unlike the RTL view or the Hierarchical Post-Synthesis view, shows only one value for fanout (global fanout) because it is a flattened view (no hierarchy).

For nets that are part of a NetBundle, the NetBundle name is followed by a number in parentheses that indicates the total number of nets in the NetBundle.

Figure 4-9. Design Tree Window



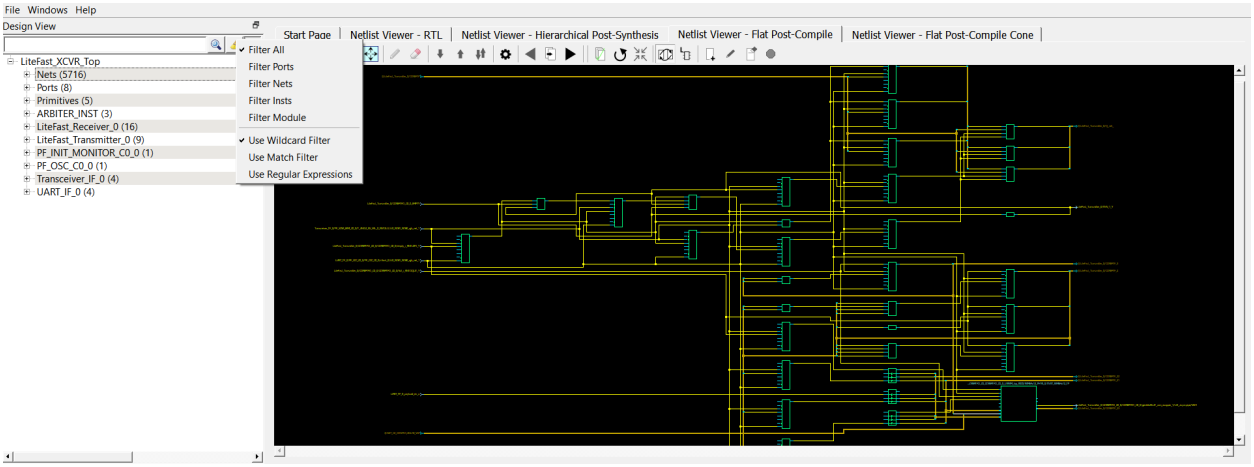
4.4.1 Filter (Ask a Question)

The display of design objects in this view can be filtered based on:

- Ports—displays all ports only, including component level ports.
- Nets—displays all nets only, including component level nets.
- Instances—displays all instances only, including component level instances.

- Modules—displays all modules only.
- Filter All—displays all design objects only.
- Use Wildcard Filter
- Use Match Filter
- Use Regular Expressions

Click the **Filter** button at the top-right corner of the Design view to filter design objects.



4.4.2 Interoperability Between Windows and Views (Ask a Question)

When a design object such as a net, an instance or a port is selected in the Design Tree window, the object is selected in the different netlist views. The reverse is also true. An object selected in one netlist view window is also selected in the Design Tree window and other netlist views.

Interoperability works only when the Toggle Cross-probing icon is enabled.

4.5 Canvas Window (Ask a Question)

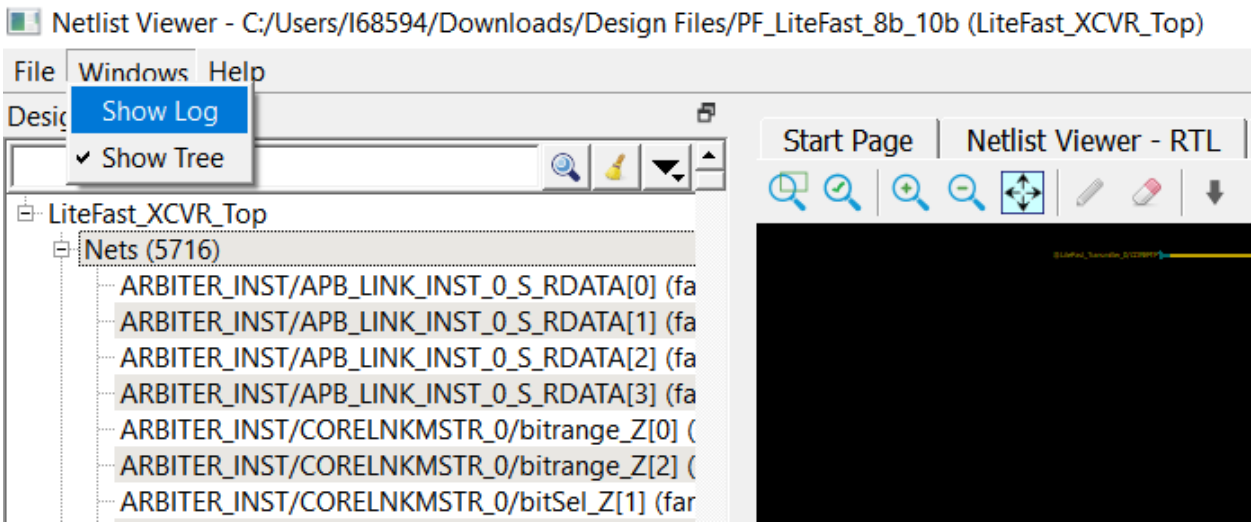
The Canvas Window displays the:

- RTL view
- Hierarchical Post-Synthesis view
- Flat Post-Compile view
- Flat Post-Compile Cone view
- Cones view
- Opened HDL files (not available in the Flat Post-Compile view)
- Start Page—when no netlist views are opened

When a view is opened, a view tab is added across the top of the Canvas window for ease of switching between views.

Important: To get a larger display area for the Canvas view, hide the Design Tree Window (**Netlist Viewer** > **Windows** > **Uncheck Show Tree**) and hide the **Log** window (**Netlist Viewer** > **Windows** > **Uncheck** > **Show Log**) Hiding the **Log** window and the **Design Tree** window leaves more display area for the **Canvas** window. Alternatively, press **CTRL+W** to maximize the work area.

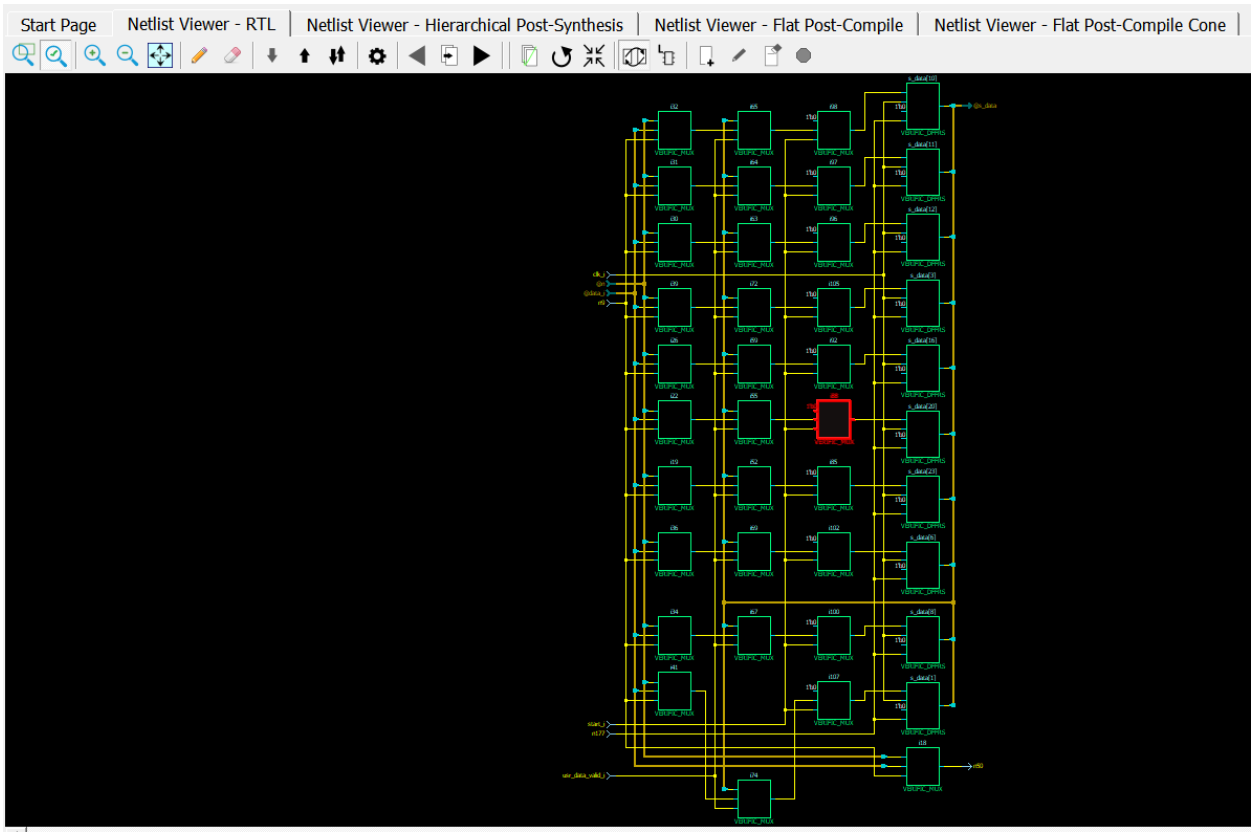
Figure 4-10. Turn on/off Design Tree Window and Log Window



Icons in the Canvas window allow you to:

- Traverse vertically up (Pop) or down (Push) the design hierarchy
- Navigate horizontally across different pages of the design view
- Zoom in/out of the design view
- Trace critical nets to the driver/load
- Create logical cones for debugging
- Control the color display the design objects

Figure 4-11. Canvas Window



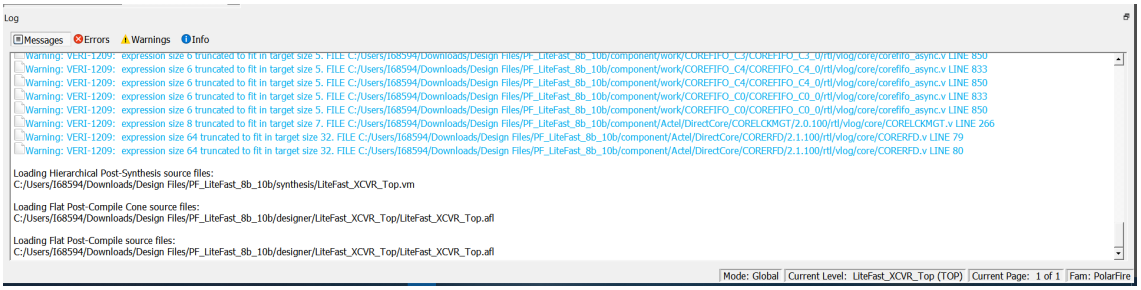
4.6 Log Window (Ask a Question)

The **Log** window displays the following:

- Informational messages such as the location and name of the files used to display the view.
- Any syntax errors in the HDL file if the HDL file is opened with the **Open File Location** option (right click design object > **Open File Location**).

Important: The **Log** window displays by default when the **Netlist Viewer** opens. Hiding the **Log** window will leave more display area for the Canvas view. To get a larger display area for the Canvas view, hide the **Log** window (**Netlist Viewer** > **Windows** and uncheck (**Show Log**).

Figure 4-12. Log Window



4.6.1 Status Bar (Ask a Question)

The status bar at the bottom-right corner of the Netlist Viewer displays the following:

- Mode—displays Global or Local mode. Global mode means the Netlist Viewer can cross hierarchical boundaries when following nets to drivers or loads. Local means the Netlist Viewer stays in the current level of design hierarchy.
- Current Level—displays the current level of design hierarchy, either TOP_LEVEL instance name or instance name of the component
- Current Page—displays the current page of the Netlist Viewer (Page x of <total>) when traversing across different pages of the Netlist Viewer
- Fam—displays the technology family

Figure 4-13. Status Bar

5. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
J	05/2023	Updated the document with the latest and better quality graphics.
H	04/2023	This document is released with Libero SoC Design Suite v2023.1 without changes from v2022.3.
G	12/2022	This document is released with Libero SoC Design Suite v2022.3 without changes from v2022.2.
F	08/2022	This document is released with Libero SoC Design Suite v2022.2 without changes from v2022.1.
E	04/2022	This document is released with Libero SoC Design Suite v2022.1 without changes from v2021.3.
D	12/2021	• In section 1. Supported Families and Platforms, added PolarFire SoC to the list of supported devices. • Updated the document with better quality graphics.
C	08/2021	This document is released with Libero SoC Design Suite v2021.2 without changes from v2021.1.
B	04/2021	Editorial updates only. No technical content updates.
A	11/2020	Document converted to Microchip template.
4.0	12/2018	Document template updates and minor text edits
3.0	10/2017	Added Flat Post-Compile Cone View
2.0	05/2017	Minor updates
1.0	12/2016	Initial Revision

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